CLAIMS:

1. A semiconductor processing method of forming a conductive projection comprising:

providing a substrate having a surface area over which a conductive projection is to be formed;

forming a conductive projection over the surface area, the projection having an upper surface and a side surface joined therewith defining a corner region; and

beveling the corner region of the conductive projection.

2. The semiconductor processing method of claim 1, wherein the surface area comprises a diffusion region, and further comprising after the beveling of the corner region, forming conductive material over the conductive projection and in electrical communication with the diffusion region.

3. The semiconductor processing method of claim 1, wherein the beveling of the corner region comprises facet etching the conductive projection.

4. The semiconductor processing method of claim 1, wherein the beveling of the corner region comprises:

unevenly doping material of the conductive projection proximate the upper and side surfaces thereof; and

etching material of the conductive projection containing greater concentrations of dopant at a greater rate than material of the conductive projection containing lower concentrations of dopant.

5. A semiconductor processing method of forming a conductive projection comprising:

forming a conductive line proximate a substrate node location with which electrical communication is desired;

forming a conductive projection over the node location, the projection having an upper surface and a side surface joined therewith defining a corner region, at least a portion of the corner region being disposed elevationally over the conductive line; and

beveling the corner region portion.

6. The semiconductor processing method of claim 5, wherein the beveling of the corner region portion comprises facet etching the corner region portion.

7. The semiconductor processing method of claim 5, wherein the beveling of the corner region comprises:

unevenly doping material of the conductive projection proximate the upper and side surfaces thereof; and

etching material of the conductive projection containing greater concentrations of dopant at a greater rate than material of the conductive projection containing lower concentrations of dopant.

8. A semiconductor processing method of forming a conductive projection comprising:

forming a pair of spaced-apart, insulated conductive lines over a substrate, the conductive lines defining a node location therebetween with which electrical communication is desired;

forming insulative material over the node location and between the conductive lines;

forming an opening through the insulative material and between the lines to proximate the node location;

forming conductive material within the opening over the node location, the conductive material having side surfaces which project away from the node location and terminate proximate an upper surface, the side surfaces and upper surface defining at least one corner region; and

beveling the corner region.

9. The semiconductor processing method of claim 8, wherein the forming of the insulative material comprises forming first and second layers of insulative material over the node location.

10. The semiconductor processing method of claim 9 further comprising planarizing the first layer of insulative material prior to forming the second layer of insulative material.

11. The semiconductor processing method of claim 9 further comprising removing the first and second layers of insulative material prior to beveling the corner region.

12. A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having an uppermost surface; and

unevenly removing material of the conductive plug to define a second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines.

13. The method of claim 12, wherein the unevenly removing material of the conductive plug comprises facet etching the conductive plug.

14. The method of claim 12, wherein the unevenly removing material of the conductive plug comprises:

unevenly doping material of the conductive plug with dopant proximate the uppermost surface, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive plug containing greater concentrations of dopant at a greater rate than material of the conductive plug containing lower concentrations of dopant.

15. The method of claim 14, wherein the unevenly doping material of the conductive plug comprises conducting an angled ion implant of the dopant.

16. The method of claim 12, wherein the forming of the conductive plug comprises forming the plug to have a central region and a corner region joined therewith, and the unevenly removing material of the conductive plug comprises removing more material from the corner region than from the central region.

17. The method of claim 12, wherein the forming of the conductive plug comprises:

forming insulative material over the node location, the insulative material having a generally planar upper surface;

forming a contact opening through the insulative material and exposing a portion of the node location;

filling the contact opening with conductive material; and

planarizing the conductive material relative to the insulative material upper surface.

18. The method of claim 17 further comprising removing the insulative material prior to removing the material of the conductive plug to define the second uppermost surface.

19. The method of claim 18, wherein the removing of material of the conductive plug comprises facet etching the conductive plug.

20. The method of claim 18, wherein the removing of material of the conductive plug comprises:

unevenly doping material of the conductive plug with dopant proximate the uppermost surface, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive plug containing greater concentrations of dopant at a greater rate than material of the conductive plug containing lower concentrations of dopant.

21. A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling a conductive plug formed over a diffusion region with which a bit line is to electrically communicate.

22. A method forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having an uppermost surface; and

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines.

23. The method of claim 22, wherein the etching of the material of the conductive plug comprises facet etching the conductive plug.

24. The method of claim 22, wherein the etching of the material of the conductive plug comprises:

unevenly doping material of the conductive plug with dopant proximate the uppermost surface, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive plug containing greater concentrations of dopant at a greater rate than material of the conductive plug containing lower concentrations of dopant.

25. The method of claim 22, wherein the forming of the conductive plug comprises:

forming insulative material over the node location;

forming a contact opening through the insulative material and exposing a portion of the node location;

forming conductive material within the contact opening; and

removing said insulative material prior to etching material of the conductive plug.

26. The method of claim 25 further comprising planarizing the conductive material.

27. The method of claim 25, wherein the forming of the insulative material over the node location comprises forming first and second layers of insulative material over the node location.

28. The method of claim 27 further comprising planarizing the first insulative layer prior to forming the second insulative layer.

29. The method of claim 27, wherein the forming of the second layer of insulative material comprises forming said second layer to have a generally planar surface over the node location, and further comprising after the forming of the conductive material, planarizing said conductive material to be substantially coplanar with the second layer surface.

30. The method of claim 29, wherein the etching of the material of the conductive plug comprises facet etching the conductive plug.

31. The method of claim 29, wherein the etching of the material of the conductive plug comprises:

unevenly doping material of the conductive plug with dopant proximate the uppermost surface, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive plug containing greater concentrations of dopant at a greater rate than material of the conductive plug containing lower concentrations of dopant.

32. A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having an uppermost surface which is defined in part by a corner region;

providing impurity into the corner region; and

etching material of the conductive plug containing greater concentrations of the impurity at a greater rate than material of the conductive plug containing lower concentrations of the impurity.

33. The method of claim 32, wherein the providing of the impurity comprises conducting an angled ion implant of the impurity.

34. The method of claim 32, wherein the forming of the conductive plug comprises forming the plug to project away from the node location a distance which is further than a distance one of the conductive lines projects away from the node location.

35. The method of claim 32, wherein the forming of the conductive plug comprises forming the plug's uppermost surface elevationally over both conductive lines.

36. The method of claim 32, wherein the forming of the conductive plug comprises:

forming an insulative material over the node location, at least a portion of the insulative material having a generally planar surface;

forming a contact opening through the insulative material and exposing a portion of the node location;

forming conductive material within the contact opening and over the insulative material; and

planarizing the conductive material sufficient to provide the uppermost plug surface to be generally coplanar with the generally planar surface portion of the insulative material.

37. The method of claim 36 further comprising removing the insulative material prior to the etching of the material of the conductive plug.

38. The method of claim 36 further comprising removing the insulative material prior to the providing of the impurity into the corner region.

39. A method of forming DRAM circuitry comprising:

forming conductive material over a substrate node location with which electrical communication with a bit line is desired, the node location being at least partially defined between a pair of conductive lines, the conductive material extending away from the substrate and having an uppermost surface disposed elevationally higher than the word lines, the conductive material having a first alignment tolerance relative to a substrate location in which a capacitor is to be formed; and

unevenly removing material of the conductive material and defining a second uppermost surface which is generally non-planar, at least a portion of which is disposed elevationally higher than the word lines, the conductive material having a second alignment tolerance relative to the substrate location which is greater than the first alignment tolerance.

40. The method of claim 39, wherein the unevenly removing material of the conductive material comprises beveling the conductive material.

41. The method of claim 39, wherein the unevenly removing material of the conductive material comprises facet etching the conductive material.

42. The method of claim 39, wherein the unevenly removing material of the conductive material comprises:

unevenly doping material of the conductive material proximate the uppermost surface thereof, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive material containing greater concentrations of dopant at a greater rate than material of the conductive material containing lower concentrations of dopant.

43. The method of claim 39, wherein the forming of the conductive material comprises:

forming insulative material over the node location;

forming a contact opening through the insulative material and exposing a portion of the node location;

forming conductive material within the contact opening and over the insulative material; and

planarizing conductive material disposed over the node location to provide the uppermost surface.

44. The method of claim 43 further comprising removing the insulative material before unevenly removing the material of the conductive material.

45. The method of claim 44, wherein the removing of the material of the conductive material comprises facet etching the conductive material.

46. The method of claim 44, wherein the removing of the material of the conductive material comprises:

unevenly doping material of the conductive material proximate the uppermost surface thereof, outermost side portions of the plug having greater concentrations of dopant than plug material therebetween; and

etching material of the conductive material containing greater concentrations of dopant at a greater rate than material of the conductive material containing lower concentrations of dopant.

add A6

add B3

add D3